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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,016	08/14/2000	Peter Ka-Fai Chow	95-332	8308

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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	8

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/637,016	CHOW ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9,10 and 12* is/are allowed.

6)☒ Claim(s) *1,2,11 and 13* is/are rejected.

7)☒ Claim(s) *3-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This is in response to amendment filed on March 9, 2004 (paper # 7). The finality of that action is withdrawn with respect to the rejection(s)of claim(s) 1-14 under USC 103 (a). However, upon further consideration, a new ground(s) of rejection is made in view of different interpretation of existing and newfound prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1,2, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman (U.S. Patent 5,898,687) and well establishing teaching of the art, and further in view of Deb (U.S. 6,172,990).

Regarding claim 1, Harriman '687 discloses a method of synchronizing transfer of frame tags to a switch fabric with the transfer of data frames to a buffer memory, the method comprising:

receiving, at a network switch port (Input ports 102; see Fig. 1), at least a portion of a data frame including layer 3 information (a conventional extraction circuit 114 that apportions each cell received at the switching fabric 110 into its constituent payload and header information fields; see col. 4, line 7-11. Also, upon receiving a cell, the switching

fabric extracts the payload data from the cell, stores it in the shared memory and records the memory address of that payload location in an address pointer; see col. 2, line 16-19. Noted that when a frame is received with a header, it must contain source and destination addresses (i.e. Layer 3) in order to translate or tagging the header),

generating a tag result corresponding to at least a portion of the data frame (an output translation function (OTF) 122 connected to the assemble circuit 116. As described herein, these translators cooperate to convert the contents of each received cell header field to a new header in connection with conventional translation methods; see col. 4, line 14-19. Noted that a tag result (i.e. new header) is generated at least a portion of a frame); and

synchronizing transfer of the tag result to a switch fabric (Assembler 110; Fig.1) with a transfer of at least a portion of the data frame to a buffer memory (Share Memory 112; Fig.1) based on a signal (output line 255 of the selector 252; see Fig. 1 and Fig.2) indicating a status of the transfer of the portion of the tag result to the switch fabric (referring to FIG. 1, the selected pointer address on line 255 is fed to the shared memory unit 112 in order to retrieve the corresponding cell payload information over line 118. The assemble circuit 116 of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. OTF 122 derives this header information in response to the connection address generated by the ITF 120. The header information is preferably stored in an output header table (not shown) of the ITF 120; see col. 7, line 56-64).

Harriman '687 does not explicitly disclose sending a signal from the buffer memory in order to synchronize.

This limitation is obvious and well known in the art. Noted that Harriman '687 discloses sending a notificator/pointor (i.e. transfer indication signal) via an output line to the share data memory buffer regarding the transfer indication of a new header (i.e. tag results) in order to synchronize at the assembler (i.e. Switch fabric). The goal of synchronizing is to avoid incorrect tagging or mis-assembling between new header and the payload data. Furthermore, Harriman '687 teaches sending a notification/pointing/signal initially to the payload data buffer memory by instructing where to begin, where the payload should be, and where the new header will be at the assembler before combining the header and the payload data. Also noted that it is also possible to send a notification/pointer/signal initially from the payload data buffer memory in order to achieve the same goal of synchronizing.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Harriman '687 as taught by well known established teaching for the purpose of synchronizing the tagging process between the data and the tag/header at the switch. The motivation being that by implementing the synchronization mechanism, it can avoid the delay of header processing and misordering/mistagging the payload data.

Harriman '687 does not explicitly disclose generation tag result by the network switch port.

This limitation is taught by Deb'990. Deb'990 discloses generation tag result (see FIG. 5A and B; Data structures) by the network switch port (see FIG. 2A, MAC 150); see col. 4, lines 4-16; note that the packets received from the physical layer are processed at MAC layer (i.e. network switch port/medium access controller), and the data structures are

indication of the contents each packet. In addition, Deb'990 discloses the receiving a data frame including layer 3 information (see FIG. 9, IP header 910 of IP switching; see col. 22, lines 46-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Harriman '687 and well-established teaching in art as taught by Deb'990 for the purpose of generating data structures of each processed packet at the port/medium controller, since Deb'990 states that by processing and generating data structures at lower layer, the upper level CPU is off load and reduce transmission delay that are typically attributed to hose CPU interrupts; see col. 4, lines 55-64 . The motivation being that by processing and generating a data structure at the port controller layer/level rather than only at upper level/layer, it can reduce the processing delay since the processing is performed on-the-fly at line rate as packets are streamed between layers.

Regarding claim 2, Harriman '687 discloses storing the portion of the data frame in the buffer memory (see Harriman '687 see col. 8, line 31-32; extracting the data portion from the data element and storing that portion in a location of memory).

Regarding claim 11, Harriman '687 discloses a network switch comprising:

a switch port (Input Port 102; Fig.1) having a port filter (a combination of Extractor unit 114 and Input Translation Function unit 120 (ITF); Fig.1) configured to receive at least a portion of a data frame including layer 3 information and to generate a tag result (a

conventional extraction circuit 114 that apportions each cell received at the switching fabric 110 into its constituent payload and header information fields; see col. 4, line 7-11. Also, upon receiving a cell, the switching fabric extracts the payload data from the cell, stores it in the shared memory and records the memory address of that payload location in an address pointer; see col. 2, line 16-19. Noted that when a frame is received with a header, it must contain source and destination addresses (i.e. Layer 3) in order to translate or tag the header),

a queue block (Share memory 112; Fig. 1) configured for transferring the data frame from the switch port to a buffer memory (extracting the data portion from the data element and storing that portion in a location of memory; see col. 8, line 31-32),

a switch fabric (Assembler 116; Fig. 1) configured for receiving the tag result and for performing a frame forwarding switching decision based on the tag result (i.e. new header) and monitoring of the transfer of the data frame (an output translation function (OTF) 122 connected to the assemble circuit 116. As described herein, these translators cooperate to convert the contents of each received cell header field to a new header in connection with conventional translation methods; see col. 4, line 14-19. Moreover, the assemble circuit 116 of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. OTF 122 derives this header information in response to the connection address generated by the ITF 120; see col. 7, line 59-65. Noted that assembler unit is responsible for forwarding the frame according to the new address/tag in the new header by communicating with OTF unit);

a synchronizing device (Output Translation Function 122 (OTF); Fig.1) configured to synchronize the transfer of the tag result to the switch fabric with the transfer of the at least a

portion of the data frame to the buffer memory based on a signal (output line 255 of the selector 252; see Fig. 1 and Fig.2) indicating a status of the transfer of the portion of the tag result to the switch fabric (referring to FIG. 1, the selected pointer address on line 255 is fed to the shared memory unit 112 in order to retrieve the corresponding cell payload information over line 118. The assemble circuit 116 of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. This header information is derived by OTF 122 in response to the connection address generated by the ITF 120. The header information is preferably stored in an output header table (not shown) of the ITF 120; see col. 7, line 56-64);

wherein the synchronization device (see Harriman '687 FIG. 1, OTF 122) storing the tag result (see FIG. 1, New header 124; see col. 7, lines 55-65; note that the new header 124 is send only after a selected pointer address 255 retrieves the payload. Thus, it is clear that the new header must be stored in OTF since it can not be send until the payload is retrieved and ready to reassemble.)

Harriman '687 does not explicitly disclose sending a signal to the buffer memory and a memory for synchronization device.

This limitation is obvious and well known in the art. Noted that Harriman '687 discloses OTF sending a notificator/pointor (i.e. transfer indication signal) via an output line to the share data memory buffer regarding the transfer indication of a new header (i.e. tag results) in order to synchronize at the assembler (i.e. Switch fabric). The goal of synchronizing is to avoid incorrect tagging or misassembling between new header and the payload data. Furthermore, Harriman '687 teaches sending a notification/pointing/signal

initially to the payload data buffer memory by instructing where to begin, where the payload should be, and where the new header will be at the assembler before combining the header and the payload data. Also noted that it is also possible for the data buffer to initially send a notification/pointer/signal to the OTF (i.e. synchronization device) regarding the transfer indication in order to achieve the same goal of synchronizing. Also, it is well known in the art that the data must be stored in a memory/buffer/storage/storing database.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Harriman '687 as taught by well known established teaching for the purpose of synchronizing the tagging process between the data and the tag/header at the switch and by utilizing a memory for data storage in synchronization device. The motivation being that by implementing the synchronization mechanism, it can avoid the delay of header processing and misordering /mistagging the payload data.

Regarding claim 13, Harriman '687 discloses a network switch comprising:

a switch port (Input Port 102; Fig.1) having a port filter (a combination of Extractor unit 114 and Input Translation Function unit 120 (ITF); Fig.1) configured to receive at least a portion of a data frame including layer 3 information and to generate a tag result (a conventional extraction circuit 114 that apportions each cell received at the switching fabric 110 into its constituent payload and header information fields; see col. 4, line 7-11. Also, upon receiving a cell, the switching fabric extracts the payload data from the cell, stores it in the shared memory and records the memory address of that payload location in an address

pointer; see col. 2, line 16-19. Noted that when a frame is received with a header, it must contain source and destination addresses (i.e. Layer 3) in order to translate or tag the header),

a queue block (Share memory 112; Fig. 1) configured for transferring the data frame from the switch port to a buffer memory (extracting the data portion from the data element and storing that portion in a location of memory; see col. 8, line 31-32),

a switch fabric (Assembler 116; Fig. 1) configured for receiving the tag result and for performing a frame forwarding switching decision based on the tag result (i.e. new header) and monitoring of the transfer of the data frame (an output translation function (OTF) 122 connected to the assemble circuit 116. As described herein, these translators cooperate to convert the contents of each received cell header field to a new header in connection with conventional translation methods; see col. 4, line 14-19. Moreover, the assemble circuit 116 of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. OTF 122 derives this header information in response to the connection address generated by the ITF 120; see col. 7, line 59-65. Noted that assembler unit is responsible for forwarding the frame according to the new address/tag in the new header by communicating with OTF unit);

a synchronizing device (Output Translation Function 122 (OTF); Fig.1) configured to synchronize the transfer of the tag result to the switch fabric with the transfer of the at least a portion of the data frame to the buffer memory based on a signal (output line 255 of the selector 252; see Fig. 1 and Fig.2) indicating a status of the transfer of the portion of the tag result to the switch fabric (referring to FIG. 1, the selected pointer address on line 255 is fed to the shared memory unit 112 in order to retrieve the corresponding cell payload information

over line 118. The assemble circuit 116 of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. This header information is derived by OTF 122 in response to the connection address generated by the ITF 120. The header information is preferably stored in an output header table (not shown) of the ITF 120; see col. 7, line 56-64);

wherein the synchronization device (see Harriman '687 FIG. 1, OTF 122) includes a state machine configured to control transferring the tag result (see FIG. 1, New header 124) to the switch fabric (see FIG. 1, assembler 116; see col. 7, lines 55-65; note that OTF sends the selected pointer address 255 in order to retrieved the corresponding cell payload information over line 118. At the same time, OTF also sends a new header information 124 to assembler. Thus, it is clear that OTF controls the transferring the new header information.

Harriman '687 does not explicitly disclose sending a signal to the buffer memory and a state machine.

This limitation is obvious and well known in the art. Noted that Harriman '687 discloses OTF sending a notificator/pointor (i.e. transfer indication signal) via an output line to the share data memory buffer regarding the transfer indication of a new header (i.e. tag results) in order to synchronize at the assembler (i.e. Switch fabric). The goal of synchronizing is to avoid incorrect tagging or misassembling between new header and the payload data. Furthermore, Harriman '687 teaches sending a notification/pointing/signal initially to the payload data buffer memory by instructing where to begin, where the payload should be, and where the new header will be at the assembler before combining the header and the payload data. Also noted that it is also possible for the data buffer to initially send a

notification/pointer/signal to the OTF (i.e. synchronization device) regarding the transfer indication in order to achieve the same goal of synchronizing. Also, it is well known in the art that controlling or processing mechanism for data must be configured and performed by a state machine or software algorithm.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Harriman '687 as taught by well known established teaching for the purpose of synchronizing the tagging process between the data and the tag/header at the switch and by utilizing a memory for data storage in synchronization device and providing a state machine to control or process of data. The motivation being that by implementing the synchronization mechanism, it can avoid the delay of header processing and misordering /mistagging the payload data.

Allowable Subject Matter

3. Claims 9, 10, 12 are allowed.
4. Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 703-308-7828. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
3/26/04

KENNETH VANDERPUYE
PRIMARY EXAMINER